EECE 310 - Lecture 14

Outline

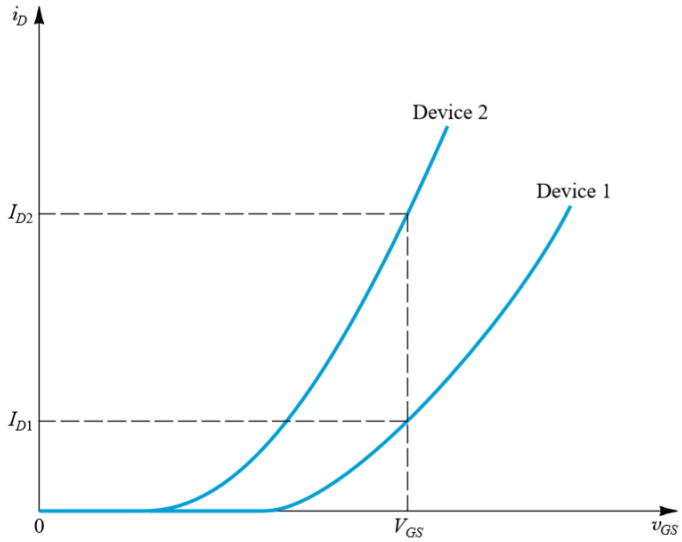
- **MOSFET Biasing**

MOSFET BIASING

- An essential step in the design of a MOSFET amplifier circuit is the establishment of an appropriate dc operating point for the transistor.
- This is known as biasing or bias design.
- An appropriate **dc operating point** or **bias point** is characterized by:
  - stable and predictable I_D
  - V_{DS} that ensures operation in the **saturation region** for all expected input

Fixing V_{GS}

- Most straightforward approach
- Fix V_{GS} to provide the desired I_D
- can be derived from V_{DD} through the use of an appropriate voltage divider
- NOT a good approach for biasing



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

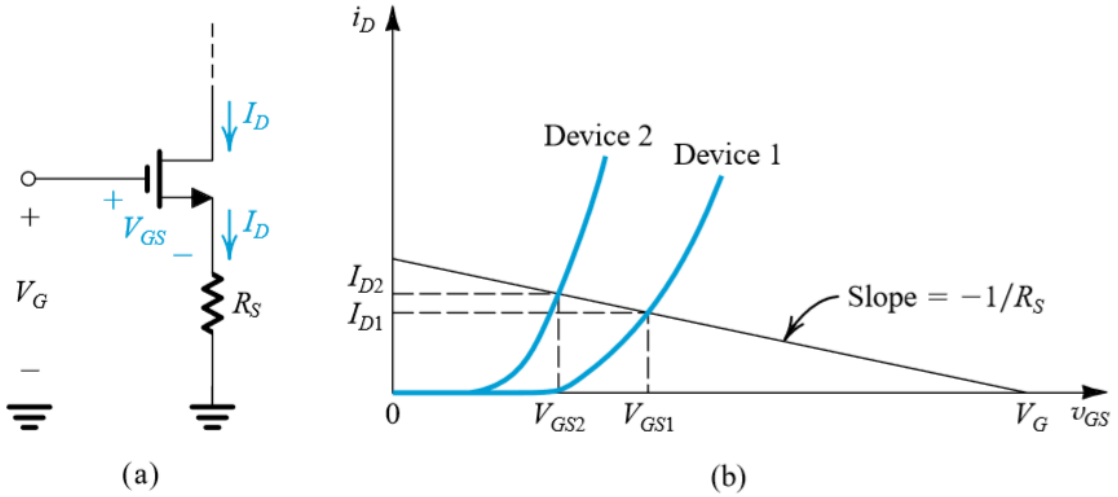
- values of V_t, C_{ox}, and (to a lesser extent) the aspect ratio vary widely among devices of supposedly the same size and type
- both V_t and μ_n depend on temperature → (if V_{GS} is fixed) I_D becomes temperature dependent
- For the fixed value of V_{GS}, the resultant spread in the values of the drain current can be substantial

Fixing V_G and Connecting a Resistance in the Source

- Excellent biasing technique

$$V_G = V_{GS} + R_S I_D$$

- The action of R_S works to keep I_D as constant as possible
- if $V_G >> V_{GS}$ → I_D will be determined by V_G and R_S
- if V_G not much larger than V_{GS} → R_S provides negative feedback and stabilizes the bias current I_D.
  - I_D increases but V_G constant → V_{GS} must decrease. → I_D decreases back to bias



Fixing V_G and Connecting a Resistance in the Source

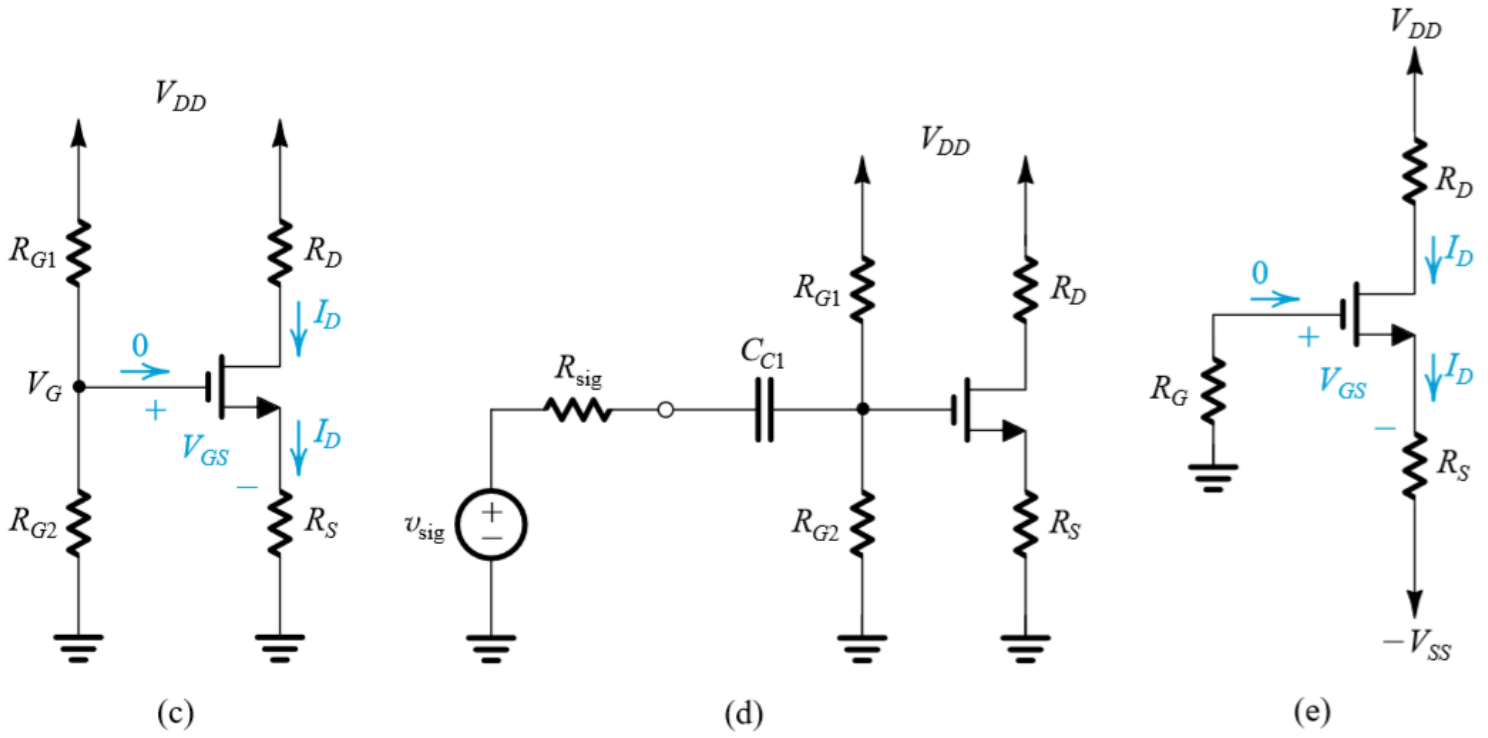


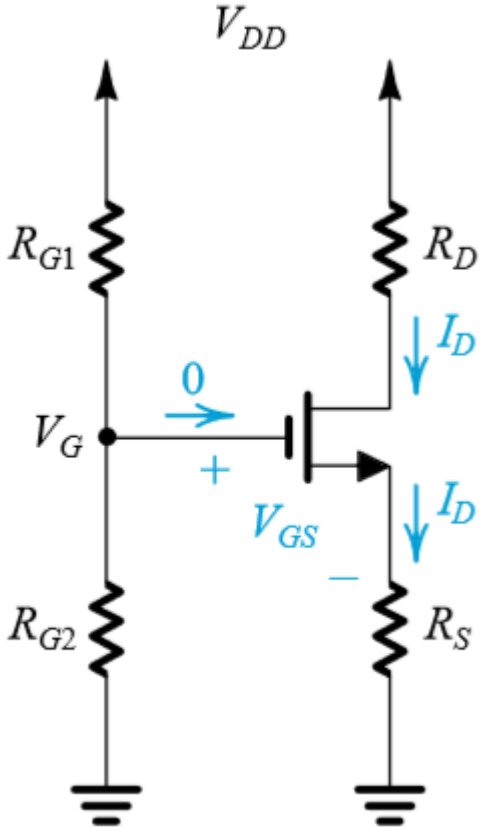
Figure 5.52 Biasing using a fixed voltage at the gate, V_G, and a resistance in the source lead, R_S: **(a)** basic arrangement; **(b)** reduced variability in I_D; **(c)** practical implementation using a single supply; **(d)** coupling of a signal source to the gate using a capacitor C_{C1}; **(e)** practical implementation using two supplies.

C_{C1} blocks dc and prevents disturbing dc bias point.

C_{C1} should be large enough to approximate a short circuit at all signal frequencies of interest

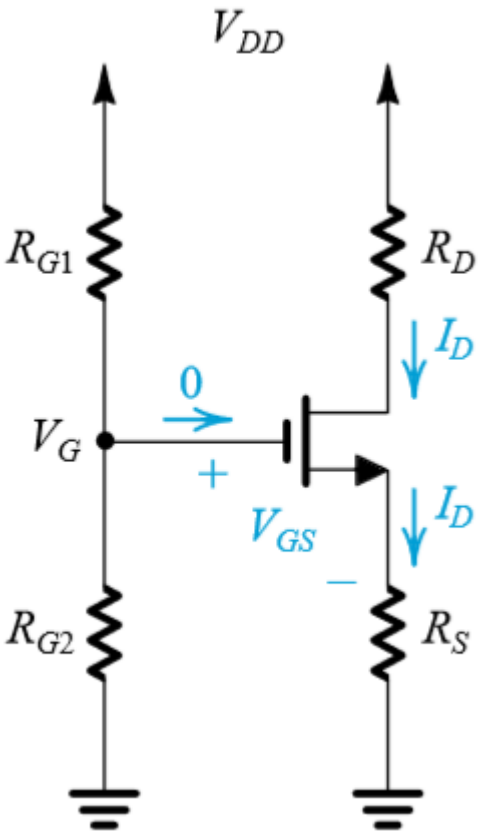
Example

- Design for I_D = 0.5 mA.
- V_t = 1 V
- V_{DD} = 15 V.
- Calculate the percentage change in the value of I_D obtained when MOSFET is replaced with another unit having the same $k'_n W/L$ but V_t = 1.5 V.



Example

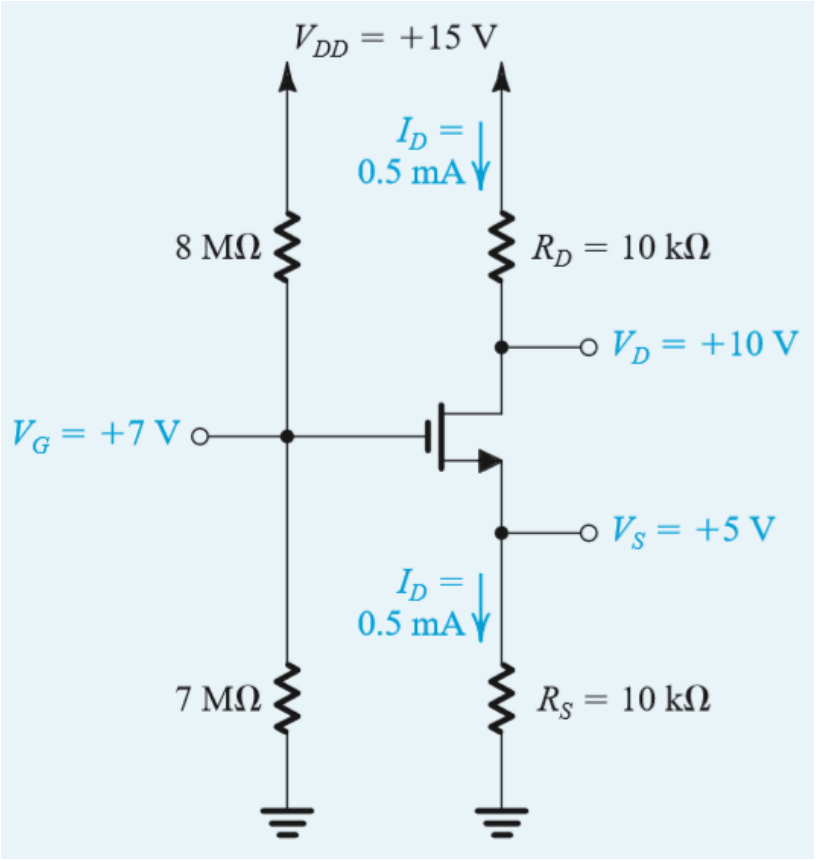
- Rule of thumb for designing this classical biasing circuit we choose R_D and R_S to provide one-third of V_{DD} as a drop across each of R_D, the transistor (i.e., V_{DS}) and R_S.
- V_{DD} = 15 V → V_S= 5V and V_D = 10 V
- → $R_D = (V_{DD}-V_D)/I_D = (15-10)/0.5$ = 10 kΩ and R_S = 5kΩ
- $I_D = ½ * k'_n (W/L)(V_{GS} - V_t)^2$ → V_{GS} = 2V
- V_G = 7V
- Choose R_{G1} = 8 MΩ and R_{G2} = 7MΩ
- Observe that the dc voltage at the drain (+10 V) allows for a positive signal swing of +5 V (i.e., up to VDD) and negative signal swing of –4 V [i.e., down to (VG – Vt)].



Example

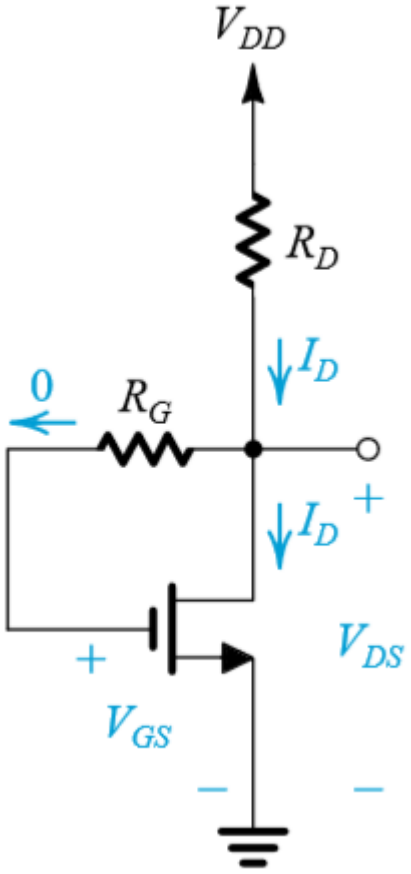
- Observe that V_D (+10 V) allows for a positive signal swing of +5 V (up to V_{DD}) and a negative signal swing of –4 V [down to $(V_G - V_t)$].
- If NMOS is replaced with another having V_t = 1.5 V
- new $I_D = ½ \times 1 \times (V_{GS} - 1.5)^2$
- But $V_G = V_{GS} + I_D R_S \rightarrow 7 = V_{GS} + 10 I_D$
- ➔ I_D = 0.455 mA
- ➔ $\Delta I_D = 0.455 - 0.5 = -0.045$ mA

which is -0.045/0.5 = -9% change



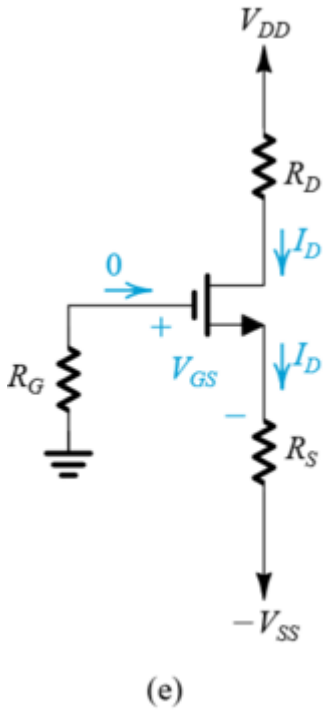
Drain-to-Gate Feedback Resistor

- Simple and effective biasing arrangement
- large feedback resistance R_G (usually in the megohm range) forces the dc voltage at the gate to be equal to that at the drain (because $I_G = 0$)
  - $V_{GS} = V_{DS} = V_{DD} - R_D I_D \rightarrow V_{DD} = V_{GS} + R_D I_D$
  - The last term is the feedback effect
- if I_D increases $\rightarrow V_{GS}$ must decrease $\rightarrow I_D$ decrease again [a change that is opposite in direction to the one originally assumed]
- Thus the negative feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible.



Circuit with two supplies

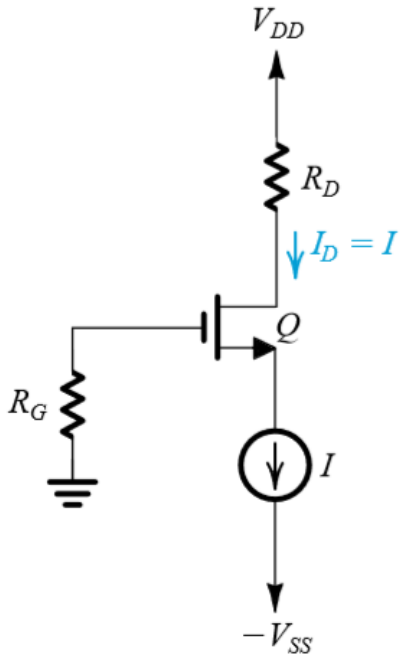
- Two voltage sources
- $V_G + V_{GS} + I_D R_D - V_{SS} = 0$
- But $V_G = 0 \rightarrow V_{GS} = V_{SS} - I_D R_D$
- Same negative feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible



(e)

Using a Constant-Current Source

- most effective scheme
- R_G (usually in the mega ohm range)
  - establishes a dc ground at the gate
  - presents a large resistance to an input signal source that can be capacitively coupled to the gate.
- Resistor R_D establishes an appropriate dc voltage at the drain to allow for the required output signal swing while ensuring that the transistor always remains in the saturation region



(a)

Using a Constant-Current Source

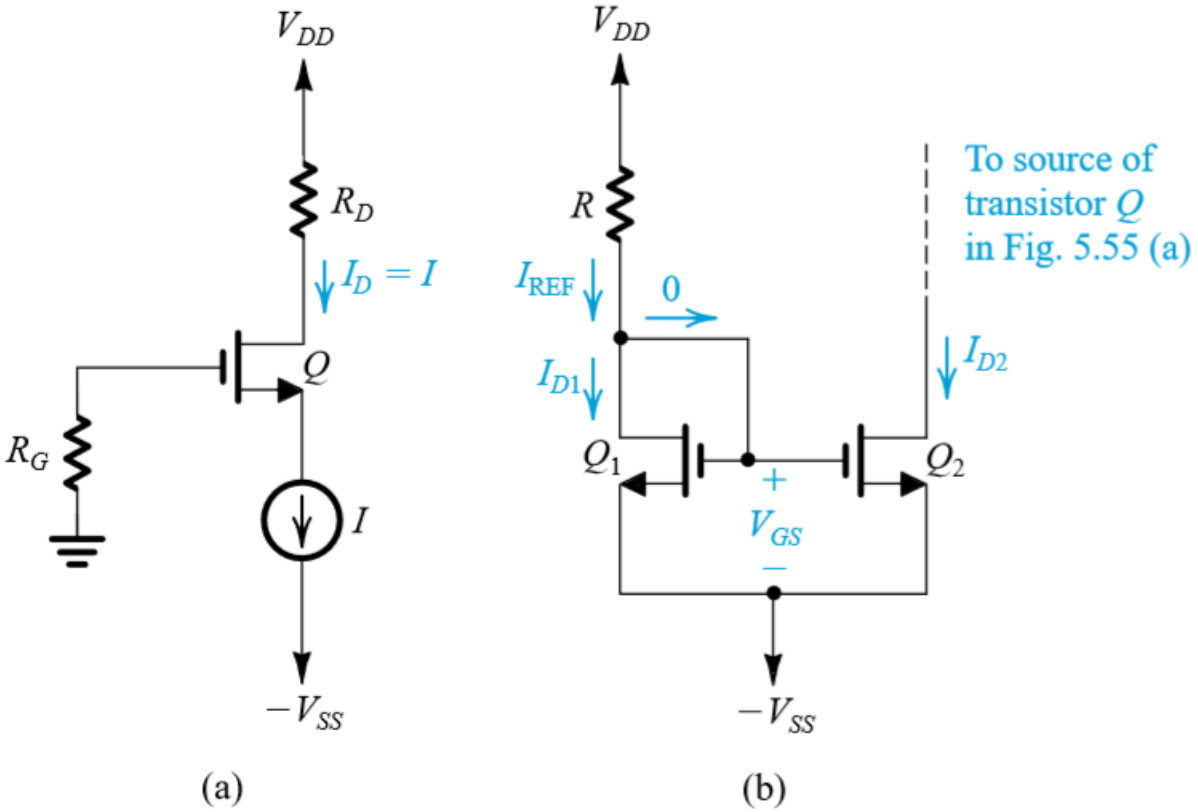


Figure 5.55 **(a)** Biasing the MOSFET using a constant-current source I. **(b)** Implementation of the constant-current source I using a current mirror.

Using a Constant-Current Source

- A circuit for implementing the constant-current source I is shown in (b).

$$I_{D1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1(V_{GS} - V_t)^2$$

$$I_{D1} = I_{\text{REF}} = \frac{V_{DD} + V_{SS} - V_{GS}}{R}$$

$$I = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2(V_{GS} - V_t)^2$$

$$I = I_{\text{REF}}\frac{(W/L)_2}{(W/L)_1}$$

- I is related to I_{REF} by the ratio of the aspect ratios of Q_1 and Q_2.
- Current mirror is very popular in the design of IC MOS amplifiers

Thank you !